Thermal and Trapping Effects in GaN-Based MESFETs

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Abstract

RF power performances of GaN-MESFETs are reported using a physics-based model that incorporates dispersion in the output resistance and transconductance due to traps and thermal effects. Calculated *I-V* characteristics are in excellent agreement with the measured results. Taking thermal effects into account the maximum output power of a 0.3μm × 100μm GaN MESFET is 22dBm at a power gain of 4.2dB at 4GHz. The corresponding quantities are 27dBm and 6.4dB, respectively if a constant channel temperature of 300K is assumed. At elevated temperatures compression in output power, gain and PAE is less in MESFETs with longer gate lengths.

Introduction

Currently, power transistors used in applications involving phased array radar and wireless base stations are Si-LDMOS which operates around 1W/mm power density range. Recently, GaN-based FETs have successfully demonstrated their usefulness in circuits operating at high temperatures, high power and high frequencies [1-4]. GaN with bandgap of 3.4eV, saturation velocity of 3×10^7 cm/s and low parasitics is suitable for high power and high frequency applications compared to Si-LDMOS and SiC-based transistors. Moreover, GaN grown on SiC offers a thermal conductivity of 4.5 W/cm/K making the system suitable for applications at high temperatures and high power. GaN HEMTs with output power of 11.7 W/mm at 10GHz with 43% power added efficiency [1], f_T = 107 GHz [2] and f_{max} = 155 GHz [3], and operating temperature of 750C [4] have been reported. However, the inability to dissipate the generated heat leads to self-heating effects [5-7]. For a GaN HFET grown on SiC, with gate width of 250μm, Nuttinck *et al.* [5] estimated the maximum temperature to be 96C in the active channel with the device operating under a continuous wave dissipation power density of 5W/mm. Due to thermal effects a 25% reduction in drain current was observed as the drain pulse width increased from 1% to 100% for the same 250μm wide GaN HFET grown on SiC [6]. Using Raman spectroscopy Kuball *et al.* [7] estimated the temperature at the gate-drain opening to be as high as 180C for a 4μm × 200μm GaN HFET grown on Sapphire at drain and gate bias of 20V and 0V, respectively.

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Self-heating effects at large drain bias increase the device lattice temperature and reduce the transport parameters such as mobility and carrier saturation velocity by increasing the carrier-phonon scattering [8,9]. Besides, GaN based devices are plagued by traps that results in performance deteriorating gate- and drain-lag transients and current collapse in the *I-V* characteristics [10, 11]. Trapping effects are dependent upon the applied signal frequency and their effect is more pronounced for frequencies less than the transconductance and output resistance dispersion frequencies [12,13]. The dispersion frequencies are related to the detrapping time constants, which are critically dependent upon the junction temperature. Therefore, an exact simulation of GaN based devices should proceed by determining the appropriate junction temperature to update the transport and detrapping parameters.

In this paper, a physics-based model is reported to determine the power performance of GaN-MESFETs by considering dispersion in the output resistance and transconductance due to traps while accounting for the thermal effects. The present treatment will allow the optimization of GaN-based MESFETs used in high power and high frequency applications.

Analysis

In the present analysis, the intrinsic and the trap related circuit parameters, as shown in Fig. 1, are obtained from a physics based analysis. Temperature and field dependent transport parameters are obtained from an ensemble Monte Carlo simulation [8, 9]. Following the treatment reported by Golio *et al.* [12] the effects of traps are incorporated through the parameters C_{ss}, g_m'' and R_{ds}''. These parameters are obtained once the underlying physical processes governing trap dynamics are formulated. Intrinsic circuit parameters: C_{gs}, C_{gd}, g_m', R_i and R_{ds}' are obtained from conventional small-signal MESFET analysis in the absence of traps and considering the effects of velocity saturation. The other circuit parameters are obtained from the reported experimental data and are as follows: $R_g = 6\ \Omega$, $L_g = 0.055$ nH, $R_d = 70\ \Omega$, $L_d = 0.307$ nH, $R_s = 90\ \Omega$, $L_s = 0.027$ nH and $C_{ds} = 0.040$ pF [11, 12].

A thermal simulator is incorporated to calculate the operating temperature for a given power level by solving Laplace's equation. The analysis proceeds with the initial guess of junction temperature to estimate mobility, carrier velocity and critical electric field for a given channel electric field to determine the drain current for given drain and gate bias. Estimating the dissipated power which is related to the product of drain voltage and current Laplace's equation is solved to obtain the updated temperature. Transport parameters and critical electric field are updated to determine the drain current and the process continues till a consistent solution in terms of drain current and temperature is obtained. The temperature

dependent transconductance and output resistance dispersion frequencies are obtained once self-consistency is achieved.

At any given frequency the overall intrinsic output conductance, g_{ds}, and transconductance, g_m, are obtained by analyzing the output subcircuit of Fig.1. For large-signal analysis, g_m, g_{ds} and C_{gs} are considered nonlinear functions of v_g while C_{gd} is nonlinear function of v_{dg}. The nonlinear functions are approximated up to second order term, $p = p_0 + p_1 v + p_2 v^2$, where p represents g_m, g_{ds}, C_{gs} or C_{gd} and v represents v_g or v_{dg}.

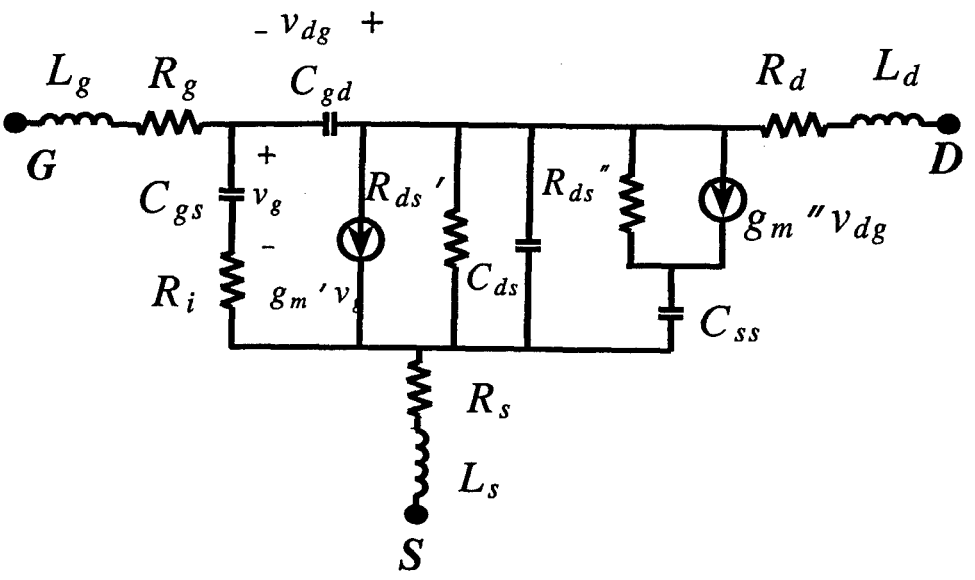

Fig.1. GaN MESFET model.

Volterra series technique is used to compute output power and nonlinearities at RF. For Volterra series analysis, the circuit shown in Fig.1 is terminated in source impedance Z_S and load impedance Z_L across the gate-source and drain-source terminals, respectively. Defining ports 1 through 5 across nonlinear elements C_{gs}, g_m and g_{ds}, C_{gd}, load and source respectively, the elements of 5 × 5 system matrix Y are expressed as follows:

$$Y_{1,1}(\omega) = 1/R_i + j\omega C_{gs0}\,, \tag{1}$$

$$Y_{1,2}(\omega) = Y_{1,3}(\omega) = Y_{3,1}(\omega) = -1/R_i\,, \tag{2}$$

$$Y_{2,1}(\omega) = -1/R_i + g_{m0}\,, \tag{3}$$

$$Y_{1,4}(\omega) = Y_{4,1}(\omega) = Y_{1,5}(\omega) = Y_{5,1}(\omega) = 0\,, \tag{4}$$

$$Y_{2,2}(\omega) = 1/R_i + \left[\left\{1/(R_d + j\omega L_d) + 1/\left(Z_s(\omega) + R_g + j\omega L_g\right)\right\}^{-1} + R_s + j\omega L_s\right]^{-1} + j\omega C_{ds} + g_{ds0}\,, \tag{5}$$

$$Y_{4,4}(\omega)=\left[\left\{1/\left(Z_s(\omega)+R_g+j\omega L_g\right)+1/\left(R_s+j\omega L_s\right)\right\}^{-1}+R_d+j\omega L_d\right]^{-1}+1/Z_L(\omega), \tag{6}$$

$$Y_{5,5}(\omega)=\left[\left\{1/\left(R_s+j\omega L_s\right)+1/\left(R_d+j\omega L_d\right)\right\}^{-1}+Z_s(\omega)+R_g+j\omega L_g\right]^{-1}, \tag{7}$$

$$Y_{2,5}(\omega)=Y_{5,2}(\omega)=-Y_{5,5}(\omega)\cdot\left[\left(R_d+j\omega L_d\right)/\left(R_s+j\omega L_s+R_d+j\omega L_d\right)\right], \tag{8}$$

$$Y_{2,4}(\omega)=Y_{4,2}(\omega)=\left[1/Z_L(\omega)-Y_{4,4}(\omega)\right]\left[\frac{Z_s(\omega)+R_g+j\omega L_g}{R_s+j\omega L_s+Z_s(\omega)+R_g+j\omega L_g}\right], \tag{9}$$

$$Y_{3,4}(\omega)=Y_{4,3}(\omega)=\left[Y_{4,4}(\omega)-1/Z_L(\omega)\right]\left[\frac{R_s+j\omega L_s}{R_s+j\omega L_s+Z_s(\omega)+R_g+j\omega L_g}\right], \tag{10}$$

$$Y_{2,3}(\omega)=Y_{3,2}(\omega)=1/R_i-Y_{2,5}(\omega), \tag{11}$$

$$Y_{3,3}(\omega)=Y_{5,5}(\omega)+1/R_i+j\omega C_{dg0}, \tag{12}$$

$$Y_{3,5}(\omega)=Y_{5,3}(\omega)=-Y_{5,5}(\omega), \text{ and} \tag{13}$$

$$Y_{5,4}(\omega)=Y_{4,5}(\omega)=-Y_{3,4}(\omega). \tag{14}$$

With an applied signal of amplitude V_{s1} at frequency ω_1, voltages across ports 1 through 4 are determined using [14]:

$$\left[V_p(\omega_1)\right]=-\left[Y_{i=p,\,j=1,\cdots,4}\right]^{-1}\left[Y_{i=p,\,j=5}\right]\left[V_{5,1,q}=V_{s1}\right] \tag{15}$$

where $p = 1,\ldots,4$. The second-order voltages appear across ports at mixing frequencies, $\omega_{2,k} = \omega_1 + \omega_2$ when two tones are applied with amplitudes V_{s1} and V_{s2} at frequencies ω_1 and ω_2, respectively. Second-order port voltages are calculated by applying nonlinear currents through each nonlinear port. The nonlinear currents are evaluated using first-order port voltages due to individual tones and p_1 coefficients of nonlinear elements [14]. With Y matrix evaluated at mixing frequencies, the second-order port voltages are given by,

$$\left[V_p(\omega_1,\omega_2)\right]=-\left[Y_{i=p,\,j=1,\cdots,4}\right]^{-1}\left[I_{i=p,2,k}\right]^T,\ p=1,\cdots,4. \tag{16}$$

Similarly, third-order port voltages due to tone amplitudes V_{s1}, V_{s2} and V_{s3} and frequencies ω_1, ω_2 and ω_3 are calculated by applying current sources due to nonlinear

coefficients p_1 and p_2 and first and second-order port voltages. The fundamental component of the output power is given by,

$$P_{out} = 0.5|V_4(\omega_1)/Z_L(\omega_1)|^2 \,\mathrm{Re}[Z_L(\omega_1)]. \tag{17}$$

Results and Discussion

Fig.2 shows calculated DC and pulsed *I-V* characteristics incorporating thermal and trapping effects for a 0.3μm × 100μm GaN MESFET [10]. Experimental results are plotted on the same figure to show good agreement [10]. The MESFET structure was grown on sapphire with a 2000 Å n-GaN active layer with doping concentration of 2.7 x 10^{17} cm^{-3} [10]. In the presence of light, the DC *I-V* measurements do not show any current collapse as the electrons captured by traps located at the channel-buffer interface and the surface (between gate-drain region) have sufficient time to be released. With pulsed input signals electrons captured by the buffer traps form a depletion region in the channel at the channel-buffer interface. Besides, surface traps also capture electrons and form a virtual gate [15] which causes drain current to decrease for a given drain bias. The effect of surface traps is incorporated by considering an additional negative gate potential due to the trapped electrons in the region between gate and drain.

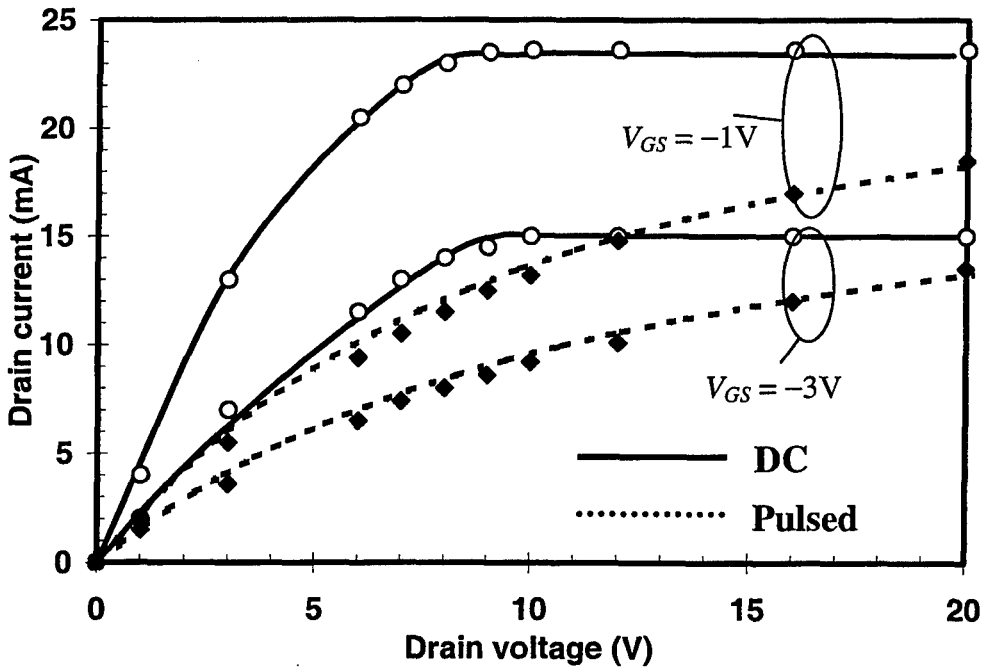

Fig.2. Calculated (solid lines) and measured (symbols) *I-V* characteristics for 0.3μm × 100μm GaN MESFET [10].

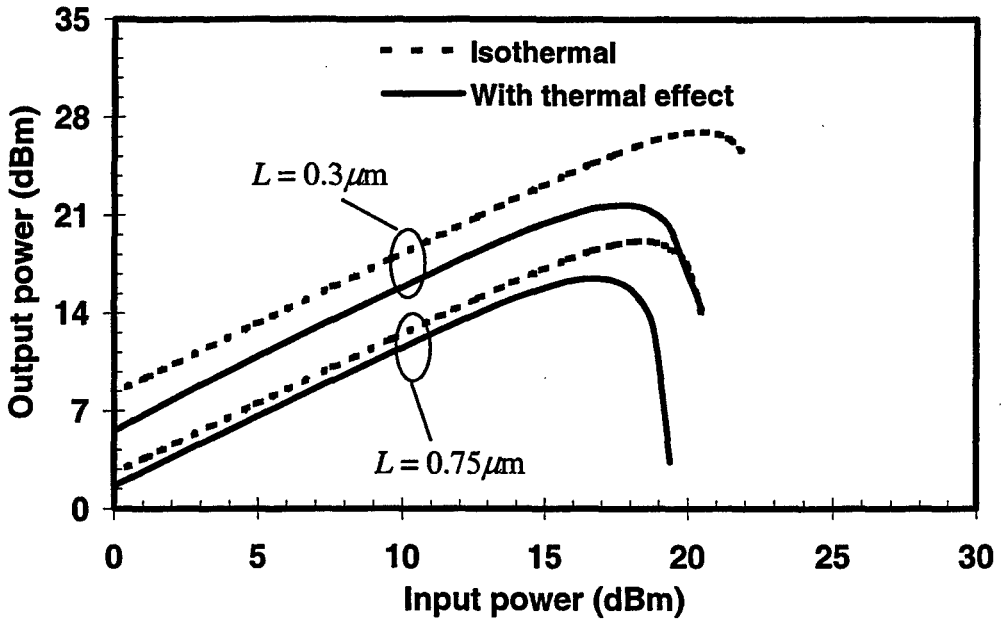

Fig.3. Variation of output power as a function of input power for $L\times100\mu$m GaN MESFET at 4GHz.

Fig.3 shows the variation of the output power as a function of input power for 0.3μm and 0.75μm gate length devices operating at 4GHz. The bias voltages are V_{GS} = -2V and V_{DS} = 30V. Using isothermal (300K) calculations maximum output powers of 27dBm and 19dBm are obtained with 0.3μm and 0.75μm gate length devices, respectively. For the same gate lengths by taking into account thermal effects the maximum output powers decrease to 22dBm and 17dBm, respectively. Higher output power is obtained for a given input power in shorter gate length devices due to higher transconductance resulting from higher differential mobility. The temperature and electric field dependent differential mobility, defined as the ratio of velocity to electric field, for the 0.3μm gate length device is given by, $\mu_n(E,T) = (1705.2 - 30.91E + 0.1564E^2) + (-3.35 + 0.075E - 4\times10^{-4}E^2)T + (0.0015 - 4\times10^{-5}E + 2\times10^{-7}E^2)T^2$, where temperature T is in K and channel electric field E is in kV/cm. Mobility expression for the 0.75μm gate length device is, $\mu_n(E,T) = (1914.4 - 36.18E + 0.1855E^2) + (-4.30 + 0.09E - 0.00053E^2)T + (0.0032 - 8\times10^{-5}E + 5\times10^{-7}E^2)T^2$. The determination of the temperature, electric field and size dependence of mobility proceeds by carrying out an ensemble Monte Carlo simulation by taking into account scatterings due to polar optical phonon, acoustic phonon, equivalent and non-equivalent intervalley scattering, impact ionization, ionized impurity, alloy, interface and self-scattering [8, 9]. For a given power

dissipation, shorter gate length devices operate at higher temperatures and their mobility and saturation velocity are greatly reduced from their corresponding room temperature values. Though, at a given temperature and electric field shorter gate length devices have a higher differential mobility as compared to devices with longer gate lengths. The higher temperature in shorter structures is due to higher dissipation power density. As a result, output power decreases significantly due to device heating in shorter structures.

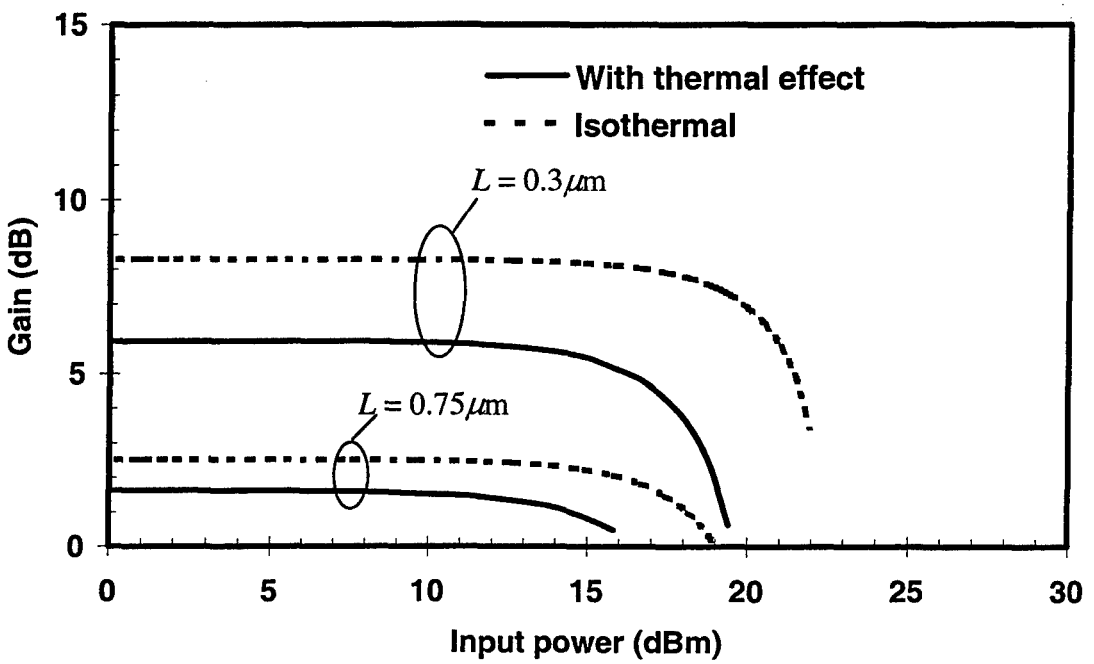

Fig.4. Variation of power gain as a function of input power for L×100μm GaN MESFET at 4GHz.

In Fig. 4, a similar result showing gain compression due to device heating is depicted. The gain compression due to thermal effects for the 0.75μm gate length device is 0.75dB. Due to higher operating temperature the gain compression for the 0.3μm gate length device is 2.2dB. Similar effects in power added efficiency (PAE) is shown in Fig.5. Shorter gate length devices have better PAE due to higher power gain. PAE compression due to thermal effects is less in longer gate length devices and follows the trend observed in output power and gain compression.

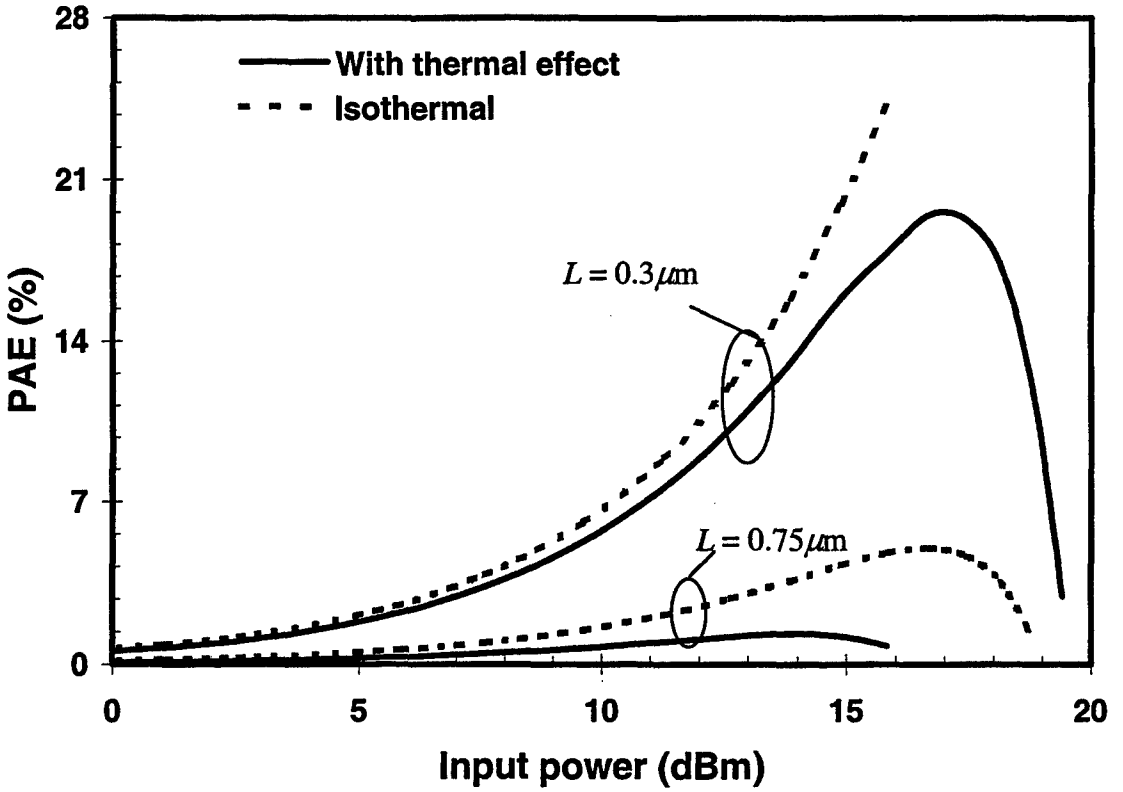

Fig.5. Variation of power added efficiency (PAE) as a function of input power for $L\times100\mu m$ GaN MESFET at 4GHz.

Conclusions

RF power performances of GaN MESFETs are analyzed considering trapping and thermal effects. The DC to RF dispersions of transconductance and output resistance due to detrapping effects and transport parameter variations with channel temperature are incorporated. Volterra series technique is used to analyze device power performance and nonlinearities. Short channel devices demonstrate higher output power, power gain and PAE, however, better thermal stability is obtained in long channel devices.

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